Marc Klingelhofer marc.klingelhofer@berkeley.edu
(650) 796-7902 linkedin.com/in/marc-klingelhofer-91710a1

Manager, Hardware/Software

Work Experience

Senior Hardware Engineer, Microsoft, Sunnyvale, CA **2/2020 – 5/2020**
- Architected and designed USB-C debug for Surface Duo (Qualcomm Snapdragon superphone)
- Developed and enforced power delivery network (PDN) constraints via SI and PCB layout
- Designed MIPI CSI-2 and DSI, I2C/I3C sensing, control, and power telemetry
- Designed bring-up and manufacturing test fixtures

Senior Software Engineer, Zola Electric, San Francisco, CA **7/2019 – 12/2019**
- Characterized power for 7.2KW solar-powered off-grid and 2.4KWH battery backup
- Improved power sharing algorithms and established shelf life
- Developed Python scripts to automate system test and characterize battery and system power
- Updated manufacturing test fixtures for programming Enphase Microinverters

Principal FPGA Engineer, Invisible Logic, Redwood City, CA **1/2019 – 6/2019**
- Datapath, control system using SystemVerilog, Vivado in high-performance Xilinx FPGAs
- Filtering and discrimination using DSP blocks
- Traffic management and collision avoidance for freight carriers
- UVM and OVM test bench, static timing analysis, floor planning, and build scripts

Senior Hardware Engineer, Boston Scientific, San Jose, CA **4/2018 – 1/2019**
- Performed failure analysis on driver boards for laser lithotripsy
- Designed and installed optical calibration tool and test fixture for production
- Designed and documented cables; scheduled deliverables with vendors

Senior Hardware Engineer, Intel, Santa Clara, CA **10/2016 – 4/2018**
- Designed hardware with Cadence Concept to validate layout guidelines for 10G/40G Ethernet, USB 3.1 Type C, DDR4 on PCIe 4.0, HDMI 2.0, OCuLink, Display Port 1.4, Thunderbolt 3.0
- Imposed electrical and physical constraints and performed placement with Allegro layout
- Simulated signal integrity, validated with time domain reflectometer (TDR)
- Provided assembly instructions and production test procedures to CM

Adjunct Professor, Cañada College, Redwood City, CA **1/2015 – 5/2017**
- Instructed Intermediate Algebra and Electronic Circuits Laboratory

Senior Hardware Engineer, Mark One Lifestyle, San Francisco, CA **11/2014 – 10/2016**
- Hardware team leader for consumer hydration monitor (drinking cup): designed schematics and performed thermal analysis; managed Allegro PCB layout of rigid-flex PCBs for fluid sensor and LED driver; designed proof-of-concept emitter/sensor arrays and developed Python to evaluate performance and accuracy of liquid sensing feature
- Designed LED and photo sensor rigid-flex circuit boards for content identification device
- Designed schematics, PCB layout of commercial LED lighting product with Infineon SoC PM DC-DC driver for 96W LED array; used spectrum analyzer to identify source of flicker
- Stood in for hardware director/VP of engineering during travel

Principal Software Engineer, HOYA ConBio & Cynosure, Fremont, CA 4/2009 – 11/2014
- Software team leader for multi-wavelength dermatological lasers compliant with IEC 82304
- Used Microsoft Team Foundation Server for version control & to track requirements/validation
- Reduced complexity of firmware to improve reliability, thereby enabling new capabilities
- Converted real-time laser controller assembly code to C, improving RS-485 and I2C operation
- Designed production test fixtures, software, and procedures

Lecturer, California State University East Bay, Hayward, CA 9/2007 – 6/2009
- Lectured Elementary and Intermediate Algebra

System Integrator, Apple, Cupertino, CA 8/2004 – 8/2007
- Used Cadence Concept and Allegro for design of Apple's original MacBook system controller, battery charger, DC-DC, power/state sequencing, accelerometer, and infrared receiver
- Developed power budget for Intel Merom chip set, LVDS/TMDS/DVI, USB, DDR, 802.11n, audio, SATA, 1000-BaseT Ethernet, LCD, system control, PCIe, 1394a (Firewire)
- Architected and verified power hierarchy and sequencing, and tested with active loads
- Assisted with CM start-up of assembly lines and validation/production procedures
- Designed power system architecture, power budgets, and sequencing for MacBook Air concept
- Designed input-output satellite board for MacBook Pro

FPGA Engineer, Pinnacle Systems, Mountain View, CA 1/2003 – 7/2004
- Introduced simulation to the design flow of a Xilinx Virtex FPGA in a broadcast video server
- Updated VHDL code to add real-time switching between multiple HD and SD video streams
- Discovered and repaired clock tree race condition

Senior ASIC Engineer, SAN Valley Systems, San Jose, CA 1/2001 – 1/2003
- Coded Verilog FIFO, 8B/10B encoder/decoder, and control for Fibre Channel/GigE gateway
- Rewrote core logic to meet timing requirements, achieving 100% timing closure while reducing device utilization from over 90% to 80% while **reducing power by** 75%
- Developed behavioral Verilog and C for unit test and system simulation
- Discovered and corrected erroneous silicon timing parameters

Senior Hardware Engineer, Omneon Video Systems, Sunnyvale, CA 10/1998 – 1/2001
- Architected PHY and link layers and switch fabric of IEEE-1394b (Firewire) packet switch
- Evaluated off-the-shelf Firewire devices and IP, choosing the most versatile and functional
- Developed RTL Verilog for a Xilinx Virtex FPGA of a dual 800Mb/s 1394b link and physical layer, including host interface, connection services, congestion management, packet generation and forwarding, topology discovery, 8B/10B encoders/decoders, and Rx/Tx rate matching
- Modelsim simulation of dual-port packet switch, with 2 FPGA-based 1394b link+PHY layers and behavioral models of a host with data generators and checkers, SerDes (serializer/deserializer) with clock recovery, and fiber transceiver with parameter-driven delay
- Automated build process with Make files, scripts for Synplify synthesis and Xilinx place-route
- Floorplanned and placed critical components and manually routed critical connections
- Performed post-synthesis, post-build static timing analysis and achieved 100% timing closure
- Debugged FPGA using oscilloscope, logic analyzer, signal generator, pattern generator

Skills

- FPGA and ASIC RTL
- Circuit, schematic, PCB
- C/C++/Python/Java/Perl/TCL source code controlled with RCS/CVS/SVN/TFS/Git/GitHub
- Verilog design of video processors, network switches/routers/packet processors, PHY/MAC
- 1Gb Ethernet/Fibre Channel/1394b Firewire/ATM (Async Transfer Mode) in FPGA and ASIC
- VHDL design of video switches and IP cores, HDTV, SDTV
- Test benches and unit test using Verilog, SystemVerilog, OVM, UVM, and VHDL
- Behavioral model of SERDES, including serialization, clock recovery, and de-serialization
- Static timing analysis and Perl build scripts
- FPGA power/reset/configuration
- High performance, low latency design, cut-through Ethernet MAC in FPGA
- Floor planning, manual routing, over-constraining critical path for timing closure
- Pipelining
- Very high-speed digital design, GHz data rate using SoC – 10G Ethernet, DDR-4, USB-C, Thunderbolt, HDMI, DisplayPort, SFP+, QSFP, PCIe
- Systems engineering, architecture, hardware/software partitioning
- Interconnects – I2C, I3C, RS-232, RS-422, RS-485, SPI, MIPI CSI/DSI, PCI, PCI-X
- PCB geometries – PCI, Eurocard, SBus, VME
- High-frequency analog and sensor design, 100MHz trans-impedance amplifiers, ADC
- Low-power (<100W) switching regulators
- Battery chargers, power switching/sequencing/delivery/distribution
- Medical system FDA 501 k premarket submission
- IEC 82304, IEC 80601 hardware/software/safety/lifecycle
- Product and test documentation
- Pre-design simulations using Spice variants and Verilog/VHDL tools
- Post-design validation using test benches – custom hardware/software and lab equipment
- Post-build verification of test procedures derived from system requirements
- Product certification, UL, CE, testing lab
- Lab work, board bring-up, debug
- Bench supplies/active loads/signal generators/oscilloscopes, logic/network/spectrum analyzers
- Identifying design defects, fault analysis, creating and validating change orders
- Designed multiple circuit boards with experimental IR/Visible/UV LED drivers and sensors
- Python test software to drive LEDs and capture sensor response via ADC
- Defined procedure, designed hardware, and evaluated liquid level sensor over 0C-100C range

Education

University of California, Berkeley, CA B.S., Electrical Engineering and Computer Science
California State University East Bay, Hayward, CA M.S., Applied Mathematics

U.S. citizen

References available upon request

Marc Klingelhofer

- Redwood City, CA, USA

Contact Information

- n1n-2e4-2tn@mail.dice.com (Preferred)
- 6507967902 (Preferred)

Work History

Total Work Experience: 30 years

- **Senior Hardware Engineer | Microsoft**
  Feb 01, 2020 - May 01, 2020
- **Firmware Engineer | Zola Electric**
  Jul 01, 2019 - Dec 01, 2019
- **Principal Engineer | Invisible Logic**
  Jan 01, 2019 - Jun 01, 2019
- **Senior Hardware Engineer | Boston Scientific**
  Apr 01, 2018 - Jan 01, 2019
- **Senior Hardware Engineer | Intel**
  Oct 01, 2016 - Apr 01, 2018
- **Adjunct Professor | Canada College**
  Jan 01, 2015 - May 01, 2017
- **Senior Hardware Engineer | Mark One Lifestyle**
  Nov 01, 2014 - Oct 01, 2016

- **Principal Firmware Engineer | Cynosure**
  Apr 01, 2009 - Nov 01, 2014 | Fremont CA United States

- **Lecturer | California State University East Bay**
  Sep 01, 2007 - Jun 01, 2009 | Hayward CA United States

- **Calculus and Literature Tutor | StudyPoint**
  Sep 01, 2007 - Jan 01, 2008 | San Francisco CA United States

- **System Integrator | Apple**
  Aug 01, 2004 - Aug 01, 2007

- **FPGA Engineer | Pinnacle Systems**
  Jan 01, 2003 - Jul 01, 2004 | Mountain View CA United States

- **Senior ASIC Engineer | SAN Valley Systems**
  Jan 01, 2001 - Jan 01, 2003

- **Senior Hardware Engineer | Omneon Video Systems**
  Oct 01, 1998 - Jan 01, 2001

- **Senior Staff Engineer | Sun**
  Oct 01, 1990 - Oct 01, 1998

Education

- **Masters**, No Dates Provided | California State University East Bay

- **Bachelors**, No Dates Provided | University of California, Berkeley

Skills

- **qa** | 28yrs | 2020
- **software engineering** | 23yrs | 2020
- **usb** | 22yrs | 2020
- **controls** | 22yrs | 2020
- **pcb** | 21yrs | 2020

- **engineering** | 19yrs | 2020
- **network** | 19yrs | 2020
- **compliance** | 18yrs | 2020
- **debugging** | 18yrs | 2020
- **i2c** | 18yrs | 2020
- **mobile devices** | 18yrs | 2020
- **electrical engineering** | 16yrs | 2020
- **software** | 16yrs | 2020
- **c** | 15yrs | 2020
- **cadence** | 15yrs | 2020
- **asic** | 10yrs | 2020
- **fpga** | 10yrs | 2020
- **verilog** | 10yrs | 2020
- **analog electronics** | 10yrs | 2020
- **embedded systems** | 8yrs | 2020
- **matlab** | 5yrs | 2020
- **systemverilog** | 5yrs | 2020
- **vhdl** | 5yrs | 2020
- **vivado** | 3yrs | 2020
- **manufacturing** | 21yrs | 2019
- **firmware development** | 6yrs | 2019
- **lasers** | 6yrs | 2019
- **hardware** | 38yrs | 2018
- **electronics** | 15yrs | 2018
- **computer graphics** | 15yrs | 2018
- **linux** | 15yrs | 2018
- **hardware development** | 14yrs | 2018
- **xilinx** | 12yrs | 2018
- **assembly** | 11yrs | 2018
- **function generator** | 9yrs | 2018
- **leadership** | 8yrs | 2018
- **product management** | 8yrs | 2018
- **scheduling** | 8yrs | 2018
- **ttl** | 8yrs | 2018
- **architecture** | 7yrs | 2018
- **allegro** | 7yrs | 2018
- **mos** | 7yrs | 2018
- **verification and validation** | 6yrs | 2018
- **python** | 4yrs | 2018
- **oscilloscope** | 9yrs | 2017
- **cm** | 5yrs | 2017
- **production** | 8yrs | 2016
- **procedure** | 7yrs | 2016
- **consumer electronics** | 5yrs | 2016
- **java** | 2yrs | 2016

- **design compiler** | 10yrs | 2014
- **synplify** | 10yrs | 2014
- **firmware** | 5yrs | 2014
- **assembly language** | 15yrs | 2011
- **video** | 14yrs | 2004
- **mpeg-2** | 8yrs | 2004
- **logic analyzer** | 10yrs | 2001
- **graphics** | 10yrs | 1998
- **atm** | 8yrs | 1998
- **project management** | 8yrs | 1998
- **sunos** | 8yrs | 1998
- **adapter** | 8yrs | 1998
- **internationalization and localization** | 8yrs | 1998
- **design**
- **internationalization**
- **localization**
- **validation**

Work Preferences

- Likely to Switch: Most Likely
- Willing to Relocate: No
- Travel Preference: Up to 25%
- Preferred Location:
    - Redwood City, CA, USA
- Work Authorization:
    - US
- Work Documents:
    - US Citizenship
- Desired Hourly Rate: 90+ (USD)
- Desired Salary: 160000+ (USD)
- Security Clearance: No
- Third Party: No
- Employment Type:
    - Full-time

Profile Sources

- Linkedin: http://www.linkedin.com/in/marc-klingelhofer-91710a1

- Dice: https://www.dice.com/employer/talent/profile/b21f1bfa4f982d1d6873efb9f97dcb6372dc74df