Rohan Madhusudan Thanki

MEM Test and Characterization Engineer

Contact Information

San Jose, CA 95134

5716357805

rthanki@mail.usf.edu

www.linkedin.com/in/rohan-thanki-1b96a4120

SKILLS SUMMARY

- Designed 2D layout and process flow of a MEMS cantilever, thermal bimorph cantilever and pressure sensor to generate 3D layout of the targeted device using CoventorWare.
- Determined device parameters such as beam displacements, stress and strain and pull-in voltage by performing mechanical, electrostatic, thermal and electro-mechanical analysis using CoventorWare.
- Hands-on experience of processing steps such as RCA wafer cleaning, proximity photolithography, wet etching and wet & dry oxidation.
- Presented a term paper to study low power system on a chip for targeted drug delivery using electrochemical mechanism for drug release**.**
- Delivered an 8 minute term paper presentation on Challenges and Solutions for High Aspect Ratio Etching of Structures.

PROJECTS

Electrical Characterization

- Characterized N-channel depletion and enhancement mode MOSFETs for saturation characteristics and capacitive behavior using HP Hewlett Packard test fixture to identify improvement opportunities.
- Calculated leakage current from breakdown current and I-V results of respective wafers and inspected the source of leakage current.
- Characterized 3 different categories of MOS capacitors with process variations using C-V, Quasi static C-V and destructive I-V measurement to perform data driven analysis of deviations and offsets of the characterization data.
- Collected 2 sets of data from 5 different sizes of MOS capacitors to plot the distribution graphs of the breakdown field and perform analysis on reported values in literature.

2-Mask NMOS fabrication in a class 1000 cleanroom

- Fabricated NMOS transistors on a (100) Si p-type wafer with a diameter of 100 mm.
- Performed RCA cleaning before each oxidation and diffusion steps in the fabrication process.
- Developed wet oxide growth by supporting oxidation furnace operation under the supervision of lab assistant.
- Operated spin coater at specified rotation speed and time to coat primer HDMS followed by positive photoresist AZ-1512 coating.
- Controlled mask aligner for proximity photolithography to align and expose wafers for printing diffusion mask pattern followed by hard bake, oxide etch using 10:1 solution of BOE and photoresist strip.
- Generated N diffusion source and drain regions through DOSE process by loading the wafers in a diffusion furnace under supervision.
- Determined sheet resistance of diffused phosphorus on control wafers by utilizing 4-probe metrology measurement.
- Observed sputtering process for aluminum metal deposition performed using a thermal evaporator.

Design of Two Input CMOS NAND Gate Process Flow

- Collaborated with a team of three students to engineer a detailed fabrication process flow for a 2 input CMOS NAND gate with 6 mask steps, N-well depth of 6 micron and N and P diffusion depths of 2 micron each.

- Generated process and device parameter calculations like wet and dry oxidation times and temperatures(to achieve a gate oxide thickness of 0.1 micron and field oxide thickness of 1 micron), N diffusion times and temperatures for dose process and drive-in diffusion, sheet resistance and drain to source current for NMOS and PMOS.
- Successfully presented a structural process flow, mask designs and an Excel Worksheet with detailed instructions for each individual process to fabricate the target device on a 100 mm wafer.

EDUCATION

University of South Florida, Tampa, FL, USA
Master of Science in Electrical Engineering, GPA 3.27/4.00, 12/2019

University of Mumbai, Mumbai, India
Bachelor of Engineering in Electronics, CGPA 6.91/10, 05/2017

CERTIFICATONS

- Learning Python, LinkedIn Learning, November 2020
- Learning C, LinkedIn Learning, October 2020
- Learning LabVIEW, LinkedIn Learning, October 2020
- Six Sigma Foundations, LinkedIn Learning, July 2020