VAISHAL SHETH

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SUMMARY

Recently Graduated MS student in Electrical and Computer Engineering with an emphasis in Communication Systems, Signal Processing and Embedded Systems from Western Michigan University. Actively Seeking a full-time position starting from January 2021.

EDUCATION

Master of Science in **Electrical and Computer Engineering** **August 2018 - December 2020**
Western Michigan University, Kalamazoo, MI, United States **GPA-3.3/4**

Bachelor of Science in **Electronics and Communication Engineering** **July 2013 - August 2017**
Gujarat Technological University, Ahmadabad, Gujarat, India **GPA-8.9/10**

Relevant Coursework: Mobile Communication, Wireless Communication, Digital Image Processing, Signal Processing, Signal and System, RF System Design, Advanced Computer Architecture, Embedded Systems, Microcontroller and Microprocessor Applications, Advanced Electronic Instrumentation.

TECHNICAL SKILLS

Programming Language: C, Python, MATLAB.
Communication Protocols: SPI, CAN, UART, I2C, ADC, DAC, PWM, Timers.
Assembly Languages: 8085, 8086, STM32F4 Microcontrollers [ARM, ARDUINO, SCILAB (basic)].
Protocols: TCP/IP, UDP, FTP, LAN, WAN.
Wireless Standards: GSM (TDMA), UMTS (W-CDMA), LTE (OFDM, MIMO), 5GNR (mmWave, Beam Forming).
Operating Systems: Linux, Windows. **Applications:** STMCUBEMX, Arduino IDE, PyCharm, LabVIEW, PSpice, LTSpice.

EXPERIENCE

Graduate Teaching/Research Assistant **January 2019 – December 2020**
Western Michigan University **Kalamazoo, MI**

- Taking Lab session of **Introduction to Microprocessors** course and solve the problems related to Machine and assembly language programming of small computers, Introduction to microcomputer architecture and interfacing.

ACADEMIC PROJECTS

1) **Behavior of OFDM System using MATLAB simulation:**
   - Implement the core signal processing blocks of the OFDM system to combat the effect of multipath reception.
   - Processing blocks of OFDM system is simulated using MATLAB for 64 subcarrier and 256 bits, tested against known Data pattern to match with the expected theoretical outcome.
2) **Simulation of Modulation Techniques:**
   - Simulation of BPSK, QPSK and 16-QAM modulation schemes were done using MATLAB comparing the robustness of each of the schemes using BER vs. SNR plot.
3) **System Level Design of Mobile Wireless User Terminal:**
   - Developing a complete system-level design for a mobile satellite-based wireless user terminal with given QPSK modulation, payload, Channel bandwidth, and burst structure.
   - Demonstration of the effect of convolution coding, puncturing, interleaving, and diversity combining.
4) **ECG measurement System:**
   - Developed a prototype of the ECG measurement system using analog circuitry and analog output converted into digital output with the help of the Arduino Mega 2560 microcontroller board.
   - Analog circuit includes Instrumentation amplifier, bandpass filter, and notch filter. The whole ECG system's circuit was made in PSpice and LTSpice and with the help of LabVIEW software and Arduino IDE showcased the ECG wave.
5) **Lane Lines Detection:**
   - lane detection algorithm begins by using ROS commands to subscribe to a ROS lane detection node that allows the camera feed to be used. Then OpenCV in Python is used for detecting the lane line through the different types of Image processing algorithms.
   - Utilizing histogram values the center lines of the lanes are calculated, and new poly fit lines are constructed over the image to create usable data for the computer. The center of the camera image is used to define the center of the vehicle so the error value can count for the PID controller.
6) **Cache Simulator for 2- level cache hierarchy**:
   - Designing and Implementing (using C) a Cache Simulator for 2-level cache hierarchy (with the optional victim cache) using Write Back (WB) write policy and Least Recently Used (LRU) replacement policy.
   - Evaluating Cache Performance in terms of Hit/Miss Rates and Average Memory Access Time (AAT) for multiple binary traces comparing different cache configuration attributes such as Set Associativity, L1/L2 Cache Sizes and Block Sizes.