# Alex Harkin

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## SUMMARY:

Highly experienced electrical engineer / hardware design engineer with experience in digital and analog designs. Interested in hardware design or field applications engineer positions.

## SKILLS:

FPGA/ASIC: Expert RTL design (with VHDL, Verilog, & System Verilog), Expert FPGA designer (Xilinx, Altera, Actel, Lattice), Excellent tools knowledge (ModelSim, Synopsis Synplify, etc.)
Processors: PowerPC (PPC), ColdFire, i.MX, 68K, ARM, x86, 8051, TI DSP, MIPS. Suppliers: Freescale, Intel, ST Micro, NXP, Texas Instruments, Analog Devices, Atmel, Microchip
Mixed Signal/Analog: Op Amps, A/D (ADC), D/A (DAC), RF amplifiers, LNA's, Mixers, sensors, MOSFETS, Transistors
Design Tools: OrCAD, Mentor Graphics, Cadence, PSpice, ViewLogic, SPECTRE, Xilinx Vivado, Altera Quartus, Lattice Diamond, Synplify Pro, Spectre, PADS, ViewLogic
Lab: Oscilloscopes, Logic Analyzers, Protocol Analyzers, Spectrum Analyzers, DMM's, VNA's, etc.
SERDES: PCI Express (PCI-e), Rapid IO (SRIO), Gigabit / 10G Ethernet (10 GbE), XAUI, HDMI, SDI
Programming: C/C++, Assembly, Linux, uCLinux
MISC: MPEG-2/4, DDR3, DDR2, PCI, VME, LVDS

## EXPERIENCE:

**Staff Hardware Design Engineer**
**Feb 2007 – Present; HP, Sunnyvale, CA**

- Work as hardware design engineer but in many instances act as field applications engineer or back up company's direct and rep partner FAE's.
- Designed large Xilinx FPGA in Verilog for interfacing with PCIExpress, Rapid IO (RIO), and 10G Ethernet to interface with network.
- Designed board for communicating/programming Xilinx and Altera FPGA's by downloading bitstream over Gigabit Ethernet link. Designed two Altera and one Xilinx FPGA for handling communication, DSP compression, interfacing, glue logic, etc.
- Designed Active Mixers (BiCMOS, 5 ~ 6 GHz & 2 ~ 4 GHz), Baseband Buffer, amplifiers, and Divider.
- Designed LCD interface board using Actel and Lattice FPGA's to drive front panel LCD's and provide communication between a PCI interface to internal MCU core. Wrote MCU code in C with inline Assembly.
- Designed PMC/XMC with a unique Front End/Back End architecture, PCIe/PCIx bridging to Dual Channel HOTLink Interfaces using Xilinx FPGA and writing complex testbenches.

- Designed and performed verification of ASIC (XIPCHIP) implemented in IBM technology (500K gates) consisting of an embedded PowerPC core, several DSP blocks, DMA subsystem, various memory and dedicated hardware interfaces, compression/decompression and image processing logic, etc.
- Designed PCB, which emulated a SOC ASIC design. The design contained a proprietary CDMA modem ASIC, an ARM7TDMI processor, DSP, HDLC processor, and other peripherals. The emulator provided a software platform for ARM processor code and DSP development prior to the SOC becoming available. Used Altera FPGAs, AHDL code, Max+Plus II, and Design Architect for PCB schematic. Performed verification of ASIC.
- Designed PLL Synthesizer (BiCMOS): VCO at 3.2 ~ 4.8 GHz, High Speed Prescaler & Divider, MA Counter, Output Buffer, Bandgap, Temperature Sensor.
- Designed a 90nm CMOS analog ASIC with multiple ADC's/DAC's, PLL's, power management, amplifier, pattern generator, health monitor, etc.
- Designed PCB using Xilinx FPGA and ARM processor to perform DSP audio compression, glue logic, interfacing, etc. Wrote complex testbenches using Verilog.
- Performed component selection and functional verification taking into considerations component reliability and availability.
- Wrote functional specifications, prepared schedules, schematic capture, component selection, writing CPLD/FPGA code, oversaw module layout, lab prototype bring-up and debug, design verification, signal integrity analysis, release to manufacturing and writing test reports.

**Principal Hardware Design Engineer**
**Jul. 2001– Jan. 2007; Oracle, San Jose, CA**

- Designed from conception through full production analog/digital circuits, DC/DC converters, sensors interface, generated schematic, prototyped, evaluated, and released products to the manufacturing.
- Designed board using DSP and Xilinx FPGA to stream in analog video, digitize it, and send out via XAUI. Board included 8051 MCU, mixed signal, power management, etc. Wrote MCU code in C and inline Assembly.
- Performed analog design with CCD imaging sensors.
- Designed board using PowerPC, Altera FPGA, ADC/DAC's, etc. to compress audio and send via Gigabit Ethernet interface.
- Designed System Box and Wiring Harness to interface PC/104+ COTS Board Stack, Altera CPLD based PC Board, Signal Connectors, Compact Flash Assembly, Switches, LEDs, and Power Distribution. Designed system Interface Cable. Generated Upper Level Signal Block Diagrams and Assembly Drawings, and supervised other engineers who performed miscellaneous tasks.
- Designed an isolated analog load cell (0-10V) and current (4-20mA) transmitter and a digital load cell amplifier.
- Designed Power Management Circuit & Multi-mode Switch & Digital Attenuator Controller (CMOS/BiCMOS/SOI): Bandgap & LDO, Oscillator, Level-shifter, Charge-pump (Negative/Positive Voltage Generation: Voltage Doubler/tripler), Digital Decoder, SPI/MIPI Interface using VHDL, RTL Compiler, & Encounter.
- Designed and VHDL coded various DSP functions (filters, interpolation, table lookup) combined with necessary controls/state machines/memory interfaces for direct hardware implementation of performance critical functions for an image reconstruction processor for a CAT Scanner implemented in FPGAs. Wrote drivers for peripherals in C.
- Managed and lead verification effort for state of the art 433 MHz 90 nm ASIC.
- Performed signal integrity experiments using oscilloscopes, logic analyzers, and spectrum analyzers to uncover complex issue with ASIC package.

- Responsible for maintaining high voltage interfaces, 380VAC/400amps 3-phase, Berkley digital PLC digital sequencers and monitoring instrumentation systems, programming of transmitter sequencers for operation of antenna and transmitter systems, audio VHF transmission between program production facility and transmitter sight and for facility air-conditioning systems to maintain adequate cooling during transmitter operation in the transmitter hall.
- Implemented test logic and performed verification for ASIC as part of XILINX FPGA (runs on PCI card in LINUX PC) and worked on LINUX device driver for this card.

**Sr. Hardware Design Engineer**
**Jul. 1995 – Jun. 2001; Northrop Grumman, Redondo Beach, CA**

- Designed board consisting of ARM processor, Xilinx FPGA, high speed DRAM, etc. to communicate via PCI/PCI-X to host system, perform data encryption, and send data out via Ethernet.
- Prepared PCB layout for good EMI performance and conducted EMI testing.
- Designed a 5:1 LRU Arbiter and verified using file based post-processing self-checking test bench in Verilog.
- Developed FPGA's and CPLD's for POTS, SONET, and power supply cards using VHDL.
- Implemented Ethernet Protocol Specifications.
- Designed mixed signal conversion daughter cards with high speed ADC/DAC's.
- Designed two modules for a synthesizer, a 50 MHz to 12GHz unit. One was a frequency divider/leveler module which received a 6.4 to 12.8GHz input from a YIG oscillator and converted it to a level controlled 50MHz to 12GHz output and the other had 12 outputs, 6 of which were 50MHz to 6GHz LO's and the other 6 were low phase noise, 8 to 100MHz, clock frequencies where the phase noise was < -152dBc/Hz at offsets from 10khz to 10MHz.
- Designed 1.333 GHz, single channel ADC/DAC (LVDS interface) Digitizer Data Recorder/Playback system.
- Designed interface card for a Wireless application, using Xilinx FPGA.
- Designed a PCI-to-SDRAM Controller, using Xilinx FPGA.
- Worked on testing high speed interfaces.
- Performed verification of ASIC in various test bench environments using PowerPC Assembler/C code at chip level.
- Designed Quad Optical SFPDP to PCI 64MHz PMC bridge residing on VME 6U platform daughter board and wrote C code and drivers.

## EDUCATION:

- Master of Science in Electrical/Computer Engineering; 1995, UCLA
- Bachelor of Science in Electrical Engineering; 1994, California Institute of Technology

# Alex Harkin

- Santa Clara, CA, USA

## Contact Information


- aharkina@yahoo.com (Preferred)
- 5103730302 (Preferred)


## Work History

### Total Work Experience: 25 years

- **Staff Hardware Design Engineer | HP**
  Feb 01, 2007 - No End Date | Sunnyvale CA United States
- **Principal Hardware Design Engineer**
  Jul 01, 2001 - Jan 01, 2007 | San Jose CA United States
- **Sr. Hardware Design Engineer | Northrop Grumman**
  Jul 01, 1995 - Jun 01, 2001 | Redondo Beach CA United States

## Skills

- **asic** | 25yrs | 2020
- **dac** | 25yrs | 2020
- **ethernet** | 25yrs | 2020
- **fpga** | 25yrs | 2020
- **interfaces** | 25yrs | 2020
- **xilinx** | 25yrs | 2020
- **pci** | 25yrs | 2020
- **engineering** | 21yrs | 2020
- **hardware development** | 21yrs | 2020
- **powerpc** | 21yrs | 2020
- **complex programmable logic device** | 21yrs | 2020
- **qa** | 21yrs | 2020
- **verification and validation** | 21yrs | 2020

- **verilog** | 20yrs | 2020
- **software** | 20yrs | 2020
- **altera** | 19yrs | 2020
- **cmos** | 19yrs | 2020
- **signal integrity** | 19yrs | 2020
- **schematic** | 19yrs | 2020
- **pcb** | 16yrs | 2020
- **qa engineering**
- **validation**

## Work Preferences

- Likely to Switch: Possibly
- Willing to Relocate: No
- Preferred Location:
    - Los Angeles, CA, USA
    - San Diego, CA, USA
    - Boston, MA, USA
- Work Authorization:
    - US
- Work Documents:
    - US Citizenship
- Security Clearance: No
- Third Party: No
- Employment Type:
    - Full-time

## Profile Sources

- Linkedin: http://www.linkedin.com/in/alex-harkin
- Dice: https://www.dice.com/employer/talent/profile/f265d7139820094bc0aee5bd5adf418707ae5002