# Stan Drey

**Cell: (256) 206-1238** **Email: sdrey@dreypm.com**
**Clearance: Active Secret**

## EXECUTIVE SUMMARY

Digital signal processing(DSP) Engineer with 25+ yrs of experience specializing in high performance computing(HPC) and signal processing employing FPGA's and GPU's.

Applications include: software defined radio(SDR), LIDAR, RADAR, medical systems, cryptography, error correction, video compression, and generally time-domain processing.

Expert in translating Matlab Models into hardware.

## EMPLOYMENT

**Pr. DSP Engineer SCIENTIFIC RESEARCH CORPORATION. Huntsville, AL**

Developed SDR and RADAR FPGA's for numerous programs.

**DSP Engineer RADIANCE TECHNOLOGIES INC. Huntsville, AL**

Developed Doppler imaging front-end for Laser ISAR system. High speed processing in CUDA on Nvidia Tesla P4 GPU's. Developed Xilinx Virtex-7 Tracker simulator w/ Fiber I/O.

**DSP/FPGA Engineer ROCKWELL COLLINS – Cedar Rapids,IA**

Waveform development for military radio products including but not limited to TTNT, JPALS, and ATDL Includes all aspects of radio functions in FPGA: doppler compensation, phase correction, encryption, error correction, mod/demod, and up/down conversion. Most work performed in both Matlab and VHDL tools.

**Consultant ROCKWELL COLLINS – Cedar Rapids,IA**

Software Defined Radio (SDR). JTRS.

**Consultant CONMED ELETROSURGERY – Denver, Co**

Developed FPGA containing DSP voltage/current/power monitoring and control of high voltage surgical cutting instrument. Spartan3/6 developed in Simulink/Sysgen tool suite.

**Consultant GENERAL DYNAMICS – Scottsdale, AZ**

Software Defined Radio (SDR). JTRS.

**Consultant DSPWORX**

Wavelet-based video compression HW/SW. FFT and wavelet compression functions implemented in Xilinx & Altera FPGA's. MATLAB used for high-level algorithm development. FPGA's synthesized with Quartus and Synplicity using VHDL. Simulation with Model Technology. Software developed in Visual C++. MPEG 2 strategic analysis.

**Consultant TERADYNE - Mnpls.**

Designed Actel FPGA in VHDL for 2Ghz AMD Gen6 processor manufacturing test equip.

**Consultant ADC TELECOMMUNICATIONS - Mnpls.**

Performed functional and static timing verification of 500K gate OFDM broadband modem ASIC. ASIC was derivative of broadband modem I previously designed for ADC. (See below)

**Consultant Intel – Chandler, AZ**

ASIC Verification.

**Sr Proj Engineer. RELTEC CORP – Dallas ,TX**

Designed HDSL transport modem board for DLC system. Transport carries (8) 292Kbaud channels across 18kft of twisted pair. Designed HDSL point to multi-point transport timing FPGA. Designed in VHDL, and targeted to Xilinx 4044XL. Designed Bus Interface FPGA. Design in VHLD and targeted to Xilinx 4013.

**Sr Proj Eng. ADC TELECOMMUNICATIONS- Mnpls,MN**

Lead Engineer of OFDM Modem development. The modem was prototyped with Xilinx and Altera FPGA's, and integrated into five LSI embedded array ASIC's. These designs were all written in VHDL, and synthesized via Synopsys & Synplicity. Designed many of the FPGA's and ASIC's used in the OFDM modem. These include equalization, QAM mod/demod, FIR Filtering, Scrambling, Differential Coding/Decoding, baseband mixers, Phase Compensation, and FFT conversions. . High-Level development/modeling performed with MATLAB and Cadence SPW.

**Sr Engineer. CYPRESS SEMICONDUCTOR -Portland,OR.**

Developer of NOVA logic simulator. NOVA was written in "C++" for MS-Windows, and ported to SUN Unix platform. Member of WARP2 development team. WARP2 is a VHDL synthesis tool used for compiling high-level VHDL designs into PLD's, FPGA's, and ASIC's. Recipient of WARP2 development achievement award. Developer of GENESIS VHDL simulator. GENESIS is a windows application written in "C++".

## EDUCATION

| | | |
|---|---|---|
| 1992 | BSEE<br>RF & DSP<br>Graduated CUM LAUDE. | Oregon Institute of Technology. |
| 2006-2008 | Financial Planning | Boston University. |

## OTHER CLAIMS TO FAME

Jaguar FFT, real-time FFT core.
High-Speed Turbo Decoder Core
Wavelet Video Compression Core

## TOOL/TECHNOLOGY PROFICIENCIES ITEMIZED

VHDL, Verilog, Synopsys, FPGA's (Altera, Xilinx, Actel, Atmel), Matlab/Simulink, Synplify DSP,Sysgen, Questasim, Vivado, Quartus, Synplicity, Quicklogic, Exemplar, SPW, Viewlogic, LSI logic ASIC's, LeonardoSpectrum. PHP, Perl, Mysql, Subversion.

## AREAS OF SPECIALIZATION

Massively Parallel DSP. FPGA/ASIC Design, Embedded DSP, Video Compression, Cryptography, Radio and Data Link Architectures.

## REFERENCES

Available to Employer Only.

# Stan Drey

- Madison, AL, USA

## Contact Information


- u4l-uyl-dv0@mail.dice.com (Preferred)
- 2562061238 (Preferred)


## Work History

### Total Work Experience: 7 years

- **Principle Engr | Scientific Research Corporation**
  Apr 01, 2019 - No End Date
- **DSP Systems Engineer | Radiance Technologies Inc.**
  Jan 01, 2018 - Apr 01, 2019
- **DSP/FPGA Engineer | ROCKWELL COLLINS**
  Nov 01, 2013 - Jan 01, 2018 | Cedar Rapids IA United States

## Skills

- **c/c++** | 25yrs | 2018
- **matlab** | 25yrs | 2018
- **dsp/software defined radio/radar/lidar** | 25yrs | 2018
- **fpga/vhdl/verilog/synplifydsp/** | 25yrs | 2018
- **gpu/cuda/opencl** | 2yrs | 2018

## Work Preferences

- Likely to Switch: Possibly
- Willing to Relocate: No
- Preferred Location:
  - Huntsville, AL, USA

- Work Authorization:
    - US
- Work Documents:
    - US Citizenship
- Desired Hourly Rate: 110+ (USD)
- Security Clearance: Yes
- Third Party: No
- Employment Type:
    - Full-time
    - Contract - Independent

## Profile Sources

- Dice: https://www.dice.com/employer/talent/profile/9af0285d150f30169d749e2f72726e2fbd77cacf