

DIVYANSHU AGRAWAL

TECHNOLOGIST

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PROFESSIONAL SUMMARY

- 10+ years for product development with 3 years of management experience
- Proven record in resolving critical program challenges under strict deadlines
- Lead development from initial concept to production using six sigma – DMAIC, DFM, DOE, FMEA, Gage r&r
- Expert on problem solving with risk assessment using 8Ds, FTA and FMEA
- Strong statistical skills for data analysis to gather insights and predict performance using JMP

EXPERIENCE

Cirrus Logic

Device Modeling Engineer, Staff

Feb 2020 – Present

- Leading random telegraphic noise characterization and modeling for MOS devices and development of Monte Carlo model with one of our Foundry partners
- Modeling of mechanical stress on semiconductor devices (MOS, passives) due to ball bump, temperature, and package
- Mechanical and equivalent spice modeling for haptics system
- Development of python-based software to analyze inline data for RTS noise monitoring

Manager, Characterization, Microphone Division

October 2016 – Jan 2020

- New development initiatives, work with external vendors to investigate new semiconductor process for simplified/more reliable product
- Communicate progress on critical initiatives with multiple cross-functional teams, track and document key takeaways, including schedules, and risk
- Lead tiger teams to solve important design/process/reliability issues
- Production test data analysis for manufacturing improvements
- Develop yield models for product parameters using Monte Carlo methodology
- Define new characterization/reliability test platforms to evaluate microphone across temperature, humidity and mechanical shock conditions.
- Managed Cirrus funded research at UT Austin, University of Athens, UCSD and applied the findings to product features
- Documentation and trainings to educate Failure analysis, Quality and Reliability, Applications and FAE teams to support customer and internal needs

Texas Instruments

MEMS Design/Integration Engineer

March 2014 – October 2016

- RF MEMS Varactor structure/package design and characterization under various environmental conditions
- Responsible for maintaining the design database, defining architecture, implementation and release of various designs, scribes for multi-factory flow, for RF MEMS program

SKILLS

Leadership • Program Management • Lean Six Sigma (DMAIC) • PDK development • Semiconductor Process • Device Physics • Validation/Characterization • NPI/ NTI • IoT

TOOLS AND PACKAGES

JMP • Spotfire • Matlab • Python • Microsoft Project • Atlassian Tools (Confluence/ JIRA) • Reliability Tests (JEDEC) • Multiphysics Modeling (Comsol, Ansys, HFSS)

EDUCATION

M.S. Electrical and Computer Engineering

Georgia Institute of Technology, Atlanta GA

GPA: 3.83

(Research Advisor: Farrokh Ayazi)

B.Tech. Electronics and Comm. Engineering

National Institute of Technology, Kurukshetra India

GPA: 4.0

(Ranked 1st in graduating class • Best Senior Design Project • Merit based tuition waiver recipient throughout undergraduate program)

- Led PDKs definition for transducer fabrication facility to ensure design guidelines are created for good Cpk
- Help evaluate transducer technologies for other groups at TI: inertial sensors, BAW resonator/filters, LiDAR
- Worked with MIT, UC Berkeley, Imperial College London, Syracuse university to help resolve issues, critical to our product development

Rotation Program Engineer

August 2011 – February 2014

5 rotations 6 months each (TI Dallas: Process Engineering, Product Development, Applications and Marketing, Characterization; TI Taiwan: Assembly and Test)

- Ran process DoEs to create material library for sensor development
- Process change investigation for particle reduction for automotive product line
- Implemented changes to improve yield at assembly and test log points to reduce cost (saving ~\$100k/year)
- Managed FACRs for pico and automotive group and various R&D programs
- Improvement/ automation to AOI process of optical projection technology
- Qualified 4 DLP pico products for consumer market
- Evaluated and published recommendations for evaluation modules from key Design Houses for various applications
- Lithography demo using DLP evaluation kit for SPIE 2014 conference

MEMS Design Engineer

August 2009 – August 2011

- Design, FEA simulation and analysis of DMD pixel architectures and non-display MEMS structures (RF MEMS, MEMS Ohmic switches, Energy Harvesting)
- Characterize devices to improve simulation methodology
- Create process and design DOEs to improve yield
- Design and characterize test structures to understand process limits

Georgia Institute of Technology

Graduate Research Assistant

January 2008 – August 2009

- Design/characterize evaluation board for vacuum-packaged tuning fork gyroscope
- Developed simplified process flow and design for a six-degree-of-freedom inertial sensor and interface circuitry in 0.6um CMOS technology
- Characterized gyroscope for sensitivity, bias stability, thermal stability and vacuum level inside the package over time
- Characterization and modeling of temperature insensitive resonators
- Wrote proposal for NSF grant for Energy harvesting using piezoelectric MEMS structures
- Designed Simulink model for IMU (Inertial Measurement Unit) based on vibratory resonant-gyroscope and accelerometer
- Physical design and layout of various MEMS structures/ test structures

REFERENCES

Available on request

PATENTS AND PUBLICATIONS

- MEMS electrostatic actuator device for RF varactor applications - US Patent numbers: 9573801, 9966194
- Micromirror apparatus and methods (TRP: new pixel architecture) - US Patent: 9348136
- High-Q Mode-Matched Vibratory Tuning Fork Based Six-Degrees of Freedom Inertial Measurement MEMS Device - US Patent: 9003882
- Design of a combined cantilever bend-torsion micro-electro-mechanical switch with increased area efficiency - Docket number: T70655
- A method to improve the switching speed and reliability of a MEMS switch - Docket number: T69182
- Gupta A, Fletcher M, Agrawal D, McMillen C, Lee J.-B., "A high dynamic restoring force actuator", Hilton Head Workshop 2012: A Solid-State Sensors, Actuators and Microsystems Workshop
- Agrawal D, "Characterization of vacuum-packaged, mode-matched, high-Q tuning fork gyroscope", Georgia Electronic Design Center (GEDC) Review Meeting 2009