SHIBAN RADHANPURI

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SUMMARY

RTL Design/Verification Engineer with 3000+ hours of hands-on experience in designing and verifying complex systems using SystemVerilog, UVM, Perl Scripting. Profound knowledge of ASIC/FPGA/SOC Design flow and Verification Methodology. In-depth knowledge of writing test plans, coverage plans, debugging RTL and Gate-Level netlists. Strong Communication skills.

TECHNICAL SKILLS

Design/Verification Languages: Verilog, SystemVerilog, C/C++
EDA/ Software Tools: Synopsys VCS, Questasim, Xilinx Vivado
Design skills: RTL Design, Timing closure, Clock Domain Crossing, OOP, FSM, ASIC/FPGA/SOC Design flow
Verification Skills: UVM, Functional Verification, Assertion based Verification- SVA, Constraint Random Coverage Driven Verification
Architecture: Branch Prediction, Out of Order Superscalar Pipeline, Instruction Level Parallelism, Cache Coherence, Multilevel Cache.

WORK EXPERIENCE

MAVEN SILICON, RTL Design and Verification, Trainee July 2020- Present

- Applied concepts like Verification flow, Self-checking testbench, Randomization, Constraints, Mailbox, Coverage, SystemVerilog Assertions.
- Managed RTL Design/Verification using SV for Verification for the following projects:

Verification Projects:

Designed and Verified Dual Port Ram [SystemVerilog, Questasim]

- Created a testbench using SystemVerilog to verify Dual port RAM functionality. Stimulus was driven by Driver to DUT.
- Implemented reference model in scoreboard and compared actual data with expected data in scoreboard.

RTL/Design/ Projects:

Design of Arbiter [SystemVerilog, Questasim]

- Designed an Arbiter for controlling 3 Processors on Questasim using Verilog/SystemVerilog. FSM was implemented in the design.
- Achieved a Code Coverage of 88% which was then improved to 100% by adding testcases.

Design of Vending Machine [SystemVerilog, Questasim]

- Designed a Vending machine on Questasim using Verilog/SystemVerilog. FSM, and 7-segment display were implemented in the design.
- Achieved a Code Coverage of 83% which was then improved to 89% by adding testcases.

Design of Digital Watch [SystemVerilog, Questasim]

- Designed a Digital watch by instantiating following sub modules for alarm clock, counter, FSM, time generator, lcd driver in the design.
- The modules were designed and functionally verified on Questasim using Verilog/SystemVerilog.

Design of 32-bit RISC-y Processor [SystemVerilog, Synopsys VCS]

- Designed a 32-bit RISC-y Processor using bottom-up methodology. The design was functionally verified on Synopsys VCS.
- Sub modules for Multiplexer, Counter, Register, ALU were instantiated in the design using Verilog/SystemVerilog.

Graduate Teaching Assistant, CSUN Jan 2019- Dec 2020

- Teaching assistant for courses like System on chip design, Digital Systems Design, Design of Digital Computers, Digital Systems and Lab.
- Lead over 120 students and solved their queries. Hold responsibility for grading quizzes and exams and leading in an assignment every week.

QUALITY FABRICATION Inc, *Internship*, Project Management, Data Analyst, Northridge, CA May 2019- Dec 2019

- Data analysis for multiple engineering departments using Excel, provided supervision to supervisors by giving direction based on analysis.
- This resulted in raising monthly turnover by 25%. Managed a team of over 50 staff and 4 supervisors with great communication skills.

ACADEMIC PROJECTS

Clean Bot Robot, ***NASA's project***, Navigation Department, CSUN July 2019- July 2020

- Designing a robot that sanitizes the NASA's floor to kill germs and microorganisms using UV led's, by avoiding flight hardware in the room.
- The SLAM algorithm helps to localize and mapping the room using data fusion of sensor data. Tools: Raspberry Pi, Technology: Python.

Ping-Pong game [FPGA, VHDL, Xilinx Vivado] Dec 2019

- Designed and simulated ping pong game using FPGA and tested on monitor using VGA controller through UART interface.
- The VGA generates the timing and synchronization signals. The movement of the ball depends on the angle of the ball hitting the paddle.

Stepper Motor [FPGA, VHDL, Xilinx Vivado] June 2019

- Controlling stepper motor in clockwise/anti-clockwise direction with DIP switches and push button. Technology: Xilinx (Vivado), VHDL.
- Used PMOD for the connection of stepper motor on Zedboard (FPGA) using UART interface.

EDUCATION

California State University Northridge, CA Master of Science, Electrical Engineering, Graduated Dec 2020 GPA: 3.6
Nirma University, India Bachelor of Engineering, Electronics & Communication Engineering, Graduated May 2018 GPA: 3.4