Parth Himanshu Pandya

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CAREER SUMMARY

- Expertise with Verilog, VHDL.
- Knowledge of scripting languages like Python.
- Hands on experience of Xilinx's Vivado, Synopsys Design Compiler, PrimeTime, TetraMAX, SDK, Questasim and Multisim.
- Experience building testbenches using Verilog, familiar with verification environment UVM.
- Understanding of Ethernet, PCIe, AXI Interface, and networking protocol TCP/IP.
- Good understanding of DFT, BIST, ATPG, JTAG and Static Timing Analysis.

EDUCATION

Master of Science in Electrical Engineering **August 2015-December 2017**
California State University, Northridge, CA, USA
Bachelor of Engineering in Electronics and Tele-Communication **August 2007-May 2011**
Shri Sad Vidya Mandal Institute of Technology, Bharuch, Gujarat, India

EXPERIENCE

Biogenex Laboratories, Fremont, CA, USA
Electrical Engineer (Field) **August 2019 - Present**

- Working on Medical IVD instruments for cancer related automated staining systems.
- Field related troubleshooting such as machine tool manufacture, installation, operation, maintenance and repair, In-house board and component level testing.
- Work with the team of Application Engineer, Manufacturing Engineer and Design Engineer

Abbott, Sylmar, CA, USA
Failure Analysis Engineer II **September 2018 – August2019**

- Troubleshooting and failure analysis of Medical Devices like Pacemaker and ICM using ATE.
- IC Testing to find the code corruption. Generate the report for reliability database.
- Knowledge of the common failure modes of electronic components and find the root cause.
- Quality engineering support using CAPA in compliance with applicable FDA and state regulations.
- Document quality issues and performance measures for management review and physicians.

ENINE Solutions, Magod, Valsad, INDIA **July 2013 - July 2015**
Design Engineer

- Developed Verilog and VHDL design codes for Xilinx FPGA.
- Simulated and verified design codes.
- Applied timing constraints to meet requirements.

- Worked with a Design team through system level verification utilizing Xilinx Vivado.
- Consulted with customers to discuss projects and products.

Elcom Door and Security Systems, Valsad, INDIA **June 2012 – July 2013**
Jr Electronics Engineer
- Experienced with digital circuit analysis, PCB design, hardware testing and debugging using ALTIUM designer.
- Worked with electrical and mechanical engineers on/off-site to complete PCB projects.
- Evaluate new product hardware designs for manufacturability and improve product designs as applicable.

PROJECTS

- **ackend Design and Testability of a Digital ASIC** **December 2017**

Using ASIC Design Synopsys's tools, Design compiler to synthesize the RoundRobin Arbiter which generates the gate-level netlists which will be used by DFT for DRC.
After that it is used by TetraMax tools for Automatic Test pattern generation for maximum Fault coverage. For Static Timing Analysis PrimeTime tool has been used.

- **Encryption and Decryption using FPGA** **December 2016**

Using a Xilinx Vertex-7 FPGA device that encrypt an incoming piece of data or data already stored in SD-Card and save that message to the SD-Card.
Afterwards, only using the correct sequence pressed on the boards button will the message be decrypted and be displayed. The encryption will be using AES or Advanced encryption standards. The button sequence password is set when the message is being decrypted.

- **FSM design Digital Lock** **December 2016**

The digital lock to be designed as user-friendly controller that receives an input sequence (password) and if that is correct, it issues a control signal to open the lock.

- **Designing of Traffic Signal in Two-way Cross Section** **May 2016**

Using FSM in VHDL coding implemented in Xilinx Vivado Design suite for testing and verification.

- **Image Compression using Different Transforms on MATLAB** **May 2011**

Transforms like DCT, BCT and Gaussian Pyramid has been implemented successfully using MATLAB.

- **LAN Network design with redundancy December 2010** Setup appropriate IP address and internet packet forwarding on the routers.

Skill Summary

Languages:	Verilog, VHDL, Python, C/C++.
Tools:	Xilinx's ISE, Vivado, HLS and SDK, Synopsys Design Compiler, TetraMAX, PrimeTime, Questasim and Modelsim, Multisim and Ultiboard, Keil and MATLAB and Microsoft Office Tools.
H/W Tools:	Logic Analyzer, Oscilloscope, Digital Multimeter and Signal Generator.
Peripheral and Protocols:	PCIe, USB, Ethernet, I2C, TCP/IP Protocols, Wishbone, and AXI Interface.
Microcontroller, FPGAs, SoC:	Xilinx Vertex 7 series FPGA, AT89C51, ARM7, Xilinx Zynq, Cypress PSoC, 8051.
Methodology/Concept:	DFT, BIST, ATPG, Static Timing Analysis, SoC and ASIC Design Flow, UVM.

Parth Pandya

- Fremont, CA, USA

Contact Information

- pandyaparth14@gmail.com (Preferred)
- 7472354515 (Preferred)

Work History

Total Work Experience: 2 years

- **Failure Analysis Engineer | Abbott**
  Sep 01, 2018 - Oct 01, 2020
- **Electrical Engineer | Biogenex Lab**
  Aug 01, 2019 - Apr 01, 2019
- **Failure Analaysis Engineer | Abbott Labs**
  Aug 01, 2018 - Feb 01, 2019 | Northridge CA United States

Education

- **Masters**, No Dates Provided | California State University Northridge

Skills

- **multimeter** | 15yrs | 2020
- **qa** | 13yrs | 2020
- **troubleshooting** | 13yrs | 2020
- **electrical engineering** | 11yrs | 2020
- **design engineering** | 6yrs | 2020
- **altium** | 6yrs | 2020
- **modelsim** | 1yrs | 2020

- **failure analysis** | 1yrs | 2019
- **design automation** | 4yrs | 2018
- **digital signal processing** | 3yrs | 2018
- **microcontrollers** | 3yrs | 2018
- **vlsi** | 3yrs | 2018
- **engineering** | 1yrs | 2018
- **ic** | 1yrs | 2018
- **iso 9000** | 1yrs | 2018
- **microsoft windows** | 1yrs | 2018
- **programming** | 1yrs | 2018
- **software** | 1yrs | 2018
- **systems design** | 1yrs | 2018
- **asic** | 3yrs | 2017
- **dft** | 3yrs | 2017
- **xilinx** | 3yrs | 2017
- **synopsys** | 2yrs | 2017
- **compiler** | 1yrs | 2017
- **business requirements** | 9yrs | 2015
- **fpga** | 7yrs | 2015
- **verilog** | 5yrs | 2015
- **implementation** | 3yrs | 2015
- **rtl** | 3yrs | 2015
- **verification and validation** | 3yrs | 2015
- **video** | 3yrs | 2015
- **cro** | 2yrs | 2014
- **digital electronics** | 2yrs | 2014
- **electronics** | 2yrs | 2014
- **logic analyzer** | 2yrs | 2014
- **optical fiber** | 2yrs | 2014
- **security** | 2yrs | 2014
- **training** | 2yrs | 2014
- **vhdl** | 2yrs | 2014
- **microprocessor** | 2yrs | 2014
- **electronic engineering** | 15yrs | 2013
- **static timing analysis** | 15yrs | 2013
- **hardware qa** | 13yrs | 2013
- **circuit analysis** | 10yrs | 2013
- **pcb** | 7yrs | 2013
- **design**
- **analysis**
- **automation**
- **validation**

Work Preferences

- Likely to Switch: Most Likely
- Willing to Relocate: Yes
- Travel Preference: Up to 25%
- Work Authorization:
    - US
- Work Documents:
    - Employment Auth Document
- Desired Hourly Rate: 40+ (USD)
- Desired Salary: 80000+ (USD)
- Security Clearance: No
- Third Party: Yes
- Employment Type:
    - Contract - W2
    - Contract to Hire - Independent
    - Full-time
    - Contract to Hire - W2
    - Contract - Independent

Profile Sources

- Linkedin: http://www.linkedin.com/in/parth-pandya-5b26a437
- Dice: https://www.dice.com/employer/talent/profile/c3fcd111b343e7312b3f0ac52736baf3e57f3d3d