MATT MOSHIR

P.O. Box 261214, San Diego, Ca. 92196

Email: mmoshir@sbcglobal.net *Cell: (619) 917-3971*

Resume date: 04/16/2020 U.S. Citizen

Senior Level FPGA Design and Development Engineer

Career preference: FPGA Development, permanent role or long term contract, W2 or 1099.
Also available for offsite or partially remote development of FPGA and Hardware, nationwide.
Preferred location: **San Diego**, California.

Summary:

- Many years of effective experience in FPGA and hardware design with demonstrated development accomplishments.
- Broad range of experience across electronics and advanced-technology industries.
- Expert in high speed, high density FPGA design and development, digital ASIC design, simulation, verification, RTL development and synthesis.
- Extensive experience and familiarity with a wide variety of hardware and software development tools both in Linux and Windows environment, FPGA and CPLD tools, schematic and layout tools, analog and digital circuit design tools, and CMOS layout tools.
- Expert in complex electronic circuits and board designs, circuit simulation, prototype, system bring-up, debug and test.
- Able to come up with quick solutions for wide range of new designs, taking advantage of resources from past experiences and design works including VHDL, Verilog, 'C' and Assembly resources.
- Clear background and able to obtain Clearance.
- Proficiency and skills in Microsoft Office tools (Word, Excel, PowerPoint, Outlook, Visio, Project).
- Holding a USPTO granted personal patent in 2012, as well as a certificate for an Advanced Altium Designer course completed in 2017.

Personal skills*:*

- Strong organizational skills and attention to details. Professional attitude and demeanor.
- Ability to multi-task in a fast-paced environment, fast learning, with short and quick ramp-up.
- Strong verbal, written, computer and technical communications.
- Ability to work independently and as a team member.
- Versatility and flexibility to work within constantly changing priorities with enthusiasm.
- Thorough understanding of electronics technologies, products, equipment, engineering concepts and practices.

Hardware skills*:*

- **Development tools:** I have designed and developed high density FPGA logic circuits using the following tools and IDEs: **Xilinx** tools: Vivado2018.2, ISE14.7**,** PlanAhead, iMPACT, PACE, Coregen, ChipScope, PinPlanner. **Altera** tools: Quartus II 10.1, SOPC Builder, Qsys, MegaWizard PLL gen., SignalTap, Component Editor. **Lattice** tools: ispLEVER, Diamond. **Simulation** tools: ModelSim PE10.4, QuestaSim64 10.4d, SynplifyPro, Simulate, Stimulus Editor and Viewer, **Misc** tools: Emacs editor, Notepad++. I have performed RTL Synthesis, Testbench development, timing analysis, emulation, debugging, simulation, verification, and worked with V-Metro modules, xdc, ucf, qsf, SFL (Serial Flash Loader), Altera Avalon I/F and AXI4, SRA, PRA bus systems.
- **Circuit design tools:** Altium Designer**,** ORCAD Sch. Capture and Layout, Pspice, PADS, PCAD**,** LTSpice.
- **Hardware languages:** Extensive familiarity and experience with VHDL, Verilog and TCL (Tool Command Language) scripts.
- **FPGAs:** Experience with **Xilinx** Virtex UltraScale+, Virtex 7/V/IV, Kintex7, Spartan 6/3, **Altera** Cyclone IV GXB**,** Stratus, Flex10K, **Lattice** Mach4000**,** as well as CPLD**,** PAL, GAL and EPCS configuration FLASH.
- **Hardware components**: I have worked with a wide variety of electronic components, transducers and sensors including: MOSFET and FET transistors, LDO, voltage regulators and switching supplies, OpAmp, Tyristor, Triac, Thermopile Laser sensor, Zener, Laser diode, LED, PIN diodes, Thermocouple,

Optocoupler, CMOS, Piezoelectric and Hall sensor, GMR, …

- **Hardware interfaces and communication techniques**: hands-on experience and familiarity with: PCIe, XAUI, USB PHY, Aurora, Ethernet, EtherCAT, RFCB (RF Control Bus), LVDS, HSS, I2C, SPI, Camera Link, DSP, PLL, VCO, DDR, ADC, DAC, IF, Baseband, PXIe, AXIe, ...
- **Lab tools**: Aerospace Test Sets with modular racks and chassis, Keysight, Tektronix and HP logic analyzer, Infiniium digital oscilloscope, spectrum analyzer, power analyzer, Signum JTAGJET**,** AVR JTAGICE, IAR jlink, Xilinx JTAG, Qualcomm CDP.

Software skills*:*

- **Processors and embedded controllers:** Developed software for Qualcomm Cell Phone MSMs including: Waverider, Aragorn and Gandalf, with ARM9, ARM7 and Cortex. Experience with Atmel Atmega, TI MSP430, PowerPc MPC860, PIC processors: PIC12C509A/PIC16F874/PIC16F887/PIC18F2525, Altera NIOS II embedded controller, OMAP.
- **Software languages**: 'C' and assembly programming in UNIX/Linux or Windows. Extensive experience with 'C' Compiler, Linker, Assembler, Make**,** Script and RTOS. Written more than 100k lines of 'C' and Assembly programs.
- **Compilers and IDEs**: Have experience with IAR IDE, AVR Studio, Microchip MPLAB**,** CCS PCW and C32 'C' Compilers, Microcross Visual X-Tools**,** winAVR, C-SPY, XLINK linker
- **Debugging and Software tools**:, EDS (Embedded Design Suite), Eclipse and BSP Editor, Chameleon ICE, FLASH programmer, Boot Loader, SAM-BA, AT commands, Teraterm, TRACE32.
- **Written device drivers for**: SDRAM, FLASH, SRAM, FIFO, EEPROM, I2C, SPI, USB, EP, Dallas 1-Wire, UART, PCI, QSFP**,** PWM, DMA, File System, Partition, Segmentation, Cluster, Sector, MBR (Master Boot Record) & PBR, FAT, Iun
- Experience with SVN (SubVersion), ClearCase, ClearQuest, Cleartool, Reflection Revision control, Citrix.

Academic Qualification: University of Science & Technology **(B.S.E.E.)** Electrical Engineering, Tehran, Iran

Experience:

Senior FPGA Development Engineer – Contract Position – Aerospace Systems – Gov. Contractor, Sep. 2018 – present

- Satellite communications systems:
  Spacecraft WMU (Wideband Modem Unit).
  Spacecraft Comm-PLY SDU (Switch Demod Unit) and CU (Control Unit) Testset.
  Missile engine control unit.
  CTU (Command Telemetry Unit), CFU (Command Formatter Unit), CSU (Command Subdecoder Unit).
  Involved with PTW and TRANSEC, including Frame formatting, Cover/Decover, AES, Permutation, Hopping, Rotation, QPSK and BMC, Modulation, Interleaving.
- Developed Ethernet PCS/PMA interface with SGMII to PHY through SelectIO LVDS I/F and with GMII to MAC for Virtex UltraScale+ FPGA on Xilinx VCU118 development platform.
- Developed Ethernet UDP Control Plane with AXI-S, MAP (Memory Access Protocol), FIFO9x4k, LinkLocal, Ethernet Frame Demux/Decoder, and Register File interfaces.
- Developed 10Gbit/s XAUI interface through GTY/GTH Transceiver, FMC+ and HTG.
- Generated 10 GbE (Gigabit Ethernet) SFP interface @ 156.25 MHz
- Developed VHDL RTL for Virtex7 UltraScale+ on Xilinx VCU118 platform and worked with Verilog IPs.
- Also developed RTL for Virtex7 on Xilinx VC707 platform.
- Created projects in Vivado 2018.2 and ISE 14.7. Compiled Xilinx libraries.
- Synthesized and Implemented designs running PAR, and generated .bit bitstream outputs.
- Instantiated and generated components and modules. Generated .xdc files and defined constraints.
- Automated simulation through .do scripts using TCL commands, Vmap, Vlib, Vcom, Vsim, wave.do … Created compile and file lists. Used Emac, Notepad++ and VI.
- Generated test bench and Stimulus with 8b10b and K-Char symbols for Ethernet packet generator and monitor. Included clock generation, clock divider, reset sync and delay functions.
- Simulated and verified the design in Linux using QuestaSim64 10.6C
- Involved in very details of BITSLICE and BITSLICE_CONTROL nibbles of SelectIO during simulation.
- Generated FIFO, XAUI with 64 bit rxd/txd and rxc/txc xgmii interface, 10Gb XGMII, ten_gig_eth_pcs_pma, and other IPs using CoreGen.
- Using Xilinx LogiCore, instantiated 10GBASE-R Ethernet PCS/PMA interface with MAC through XGMII on one end and PHY (PMD – Physical Medium Dependent) on the other.

- Worked with Exceed-On-Demand, TortoiseSVN, Office tools and lab tools.
- Generated VHDL Entity, Architecture, process, procedure and function.
- Developed VHDL in ISE 14.7 using CoolRunner II CPLD
- Developed SPI Master and Slave modules. Designed several FSM engines with Register access

Senior FPGA Development Engineer – Contract Remote Position – CurtissWright, Jul. 2017 – Nov. 2017

- Developed VHDL and Verilog RTL code for Boeing SDR (Software Defined Radio). Integrated PCIe Gen2/Gen3 x8/x4 interfaces into HDK for VPX3 with Xilinx Virtex7 FPGA in Vivado 2015.4 IDE. Instantiated Aurorax4 64B/66B core with AMBA AXI4 Stream and Frame interface. Created and integrated FusionXF Capability framework, with SRA interface. Used Vivado Power Analysis and XPE (eX Power E) tools for power analysis. Developed and integrated heater function with BRAM and DSP Slices. Created interfaces for HSS LVDS, with LVTTL user I/Os and GTX/GTP running at 5.0 Gbps. Created design hierarchy through TCL scripts and structure modules. Integrated FPGA Heater Function into HDK. Developed interface for XADC temperature and voltage monitor with I2C I/F. Integrated ADC and DAC interfaces, along with Checker and Generator. Integrated DRS SI9172 VPX3 Tuner with Aurora interface into XF07-523 XMC card. Created register map and made connections and access through FusionXF Capability. Created demo slide document in ppt. Wrote user manual.
- Created testbenches and test scripts for Chipscope_SRA and PCIe accesses through SDK and Host. Developed, instantiated and simulated NWL (NorthWest Logic) PCIe BFM interface. Simulated designs with Metro Graphic Questasim64_10.4d, as well as ModelSim PE 10.4. Used TCL for simulation.
- Compiled Xilinx libraries. Created project through TCL scripts. Also used TCL for compiling design libraries. Built, synthesized, placed, routed and implemented design, through TCL scripts and batch mode, and generated bitstream .bit FPGA image. Created Filelists and type Records in pkg modules. Defined Generics and Constants in Verilog and VHDL modules. Created design file structure hierarchy and libraries including synthesis, implementation, vm libs, source and constraints paths. Defined environment variables and managed licenses. Integrated XDC and UCF constraint files through TCL commands.
- Created and integrated interfaces for DMA engine, DDR3 SDRAM, FIFO, C2S (Card to System), S2C (System to Card) and high speed SerDes. Developed interfaces to Board Support IP (BSIP) containing PCIe, DMA Engine and MTTE. Used FPGA resources LUT, CLB, FF, DSP, Slice, Tiles.

Senior Electrical Engineer – Personal Research and Activities – San Diego, CA. Apr. 2016 – Jul. 2017

- Participated in an Advanced Altium designer course provided by Altium and obtained a certificate in 2017. In that advanced course, I learned or refreshed my experience about the subjects including, but not limited to: Differential Pair Routing, High Speed Design, Length Tuning and Calculations, Impedance Controlled Design, Design Directives, Polygons, Hierarchies, Project Management, rigid-flex PCB, Board Shape Design, Layer Stacks, Netlist, Placement, PCB Panel, Design Rules, Clearance Rules, DRC, Blanket, Classes, Nets, Rats Nests, Query Helper, Query Builder, 3D, Keepout, Cutout, Vertices, Via Stitching, Track Slicing, Teardrops, Testpoints, Assembly and Fabrication Testing, Pad and Via, Legend, Drill Pairs, Graphic Images, Logo, Barcode, Design Views, Output Job Generation, Gerber, Embedded Board Array, Inspector Panel, V-Score, V-Groove, Grids, Sheets, Template, Title Block, Mechanical Layers, Schematic and Layout Libraries, BOM, Project Management, Version Control, SVN, Repository, …
- Research and experiments with nVidia Jetson TX1 HDK carrier board, including Tegra CPU, GPUs, DDR3, USB3/2, HDMI, SD Card, PCIe, DSI, eDP, CSI, Ethernet, GPIO, JTAG and other interfaces.

Senior Electrical Engineer – Contract Position – Covidien, Carlsbad, CA. Aug. 2015 – Apr. 2016

- Designed and Developed control board circuits in Altium Designer 15, including both layout and schematic circuits such as: USB 2.0 ULPI PHY HOST controller, USB HUB, Ethernet I/F, OMAP, DVI and HDMI interfaces and control circuits, EEPROM SPI and I2C interfaces, FLASH memory, LPDDR SDRAM, UART, ESD Filters and Level Translation solutions, LDO and Buck Regulators.
- Proficient and skilled in very details of Altium IDE tool suite. Generated Fab and Assembly output files, and documented them in Agile system.
- Troubleshooting root cause of failures as in JIRA tasks. Participated in design reviews and meetings. Passed many medical devices trainings as well as FDA courses and received many certificates. Loaded and configured BL (Boot Loader), OS (Operating System) and Application programs to control boards through MMC based Debug board, TeraTerm and utility programs, using SD card and FLASH.
- Worked with QuestaSim, ModelSim, Quartus, Virtex-7 FPGA, and Office Tools.

Research and Development – personal project – San Diego, CA. Jan. 2014 – Aug. 2015

- Development, implementation and prototyping of a patent granted to me in 2012 by USPTO.
- Wrote, synthesized, programmed and tested VHDL modules in Lattice ispLEVER environment and prototyped the design using ispMACH4000. Simulated modules in ModelSim PE. Designed and

developed CMOS Layout in Electric environment.

- Developed 'C' and "Assembly" programs in MPLAB for Microchip PIC18F2525 and PIC16F883.

Senior Electrical Engineer – Contract Position – Qualcomm, San Diego, CA. Jul. 2012 – Jan. 2014

- Integration and verification of Qualcomm MSM chips including Waverider, Aragorn and Gandalf.
- Wrote 'C' source code and CMM scripts in Linux for KPSS (Krait Sub-system - ARM7/9 based controller), SPDM (System Profiling and Diagnostic Monitor), and VI automated regression routines.
- Created and managed ClearCase View, Task, Activity, Elements, Checkout and checkin.
- Worked with Trace32 Debugger, Veloce, CMM scripts, QSPR (Qualcomm Sequence Profiling Resource), Qwebstats (Qualcomm's web-based test reporting system), ClearCase, ClearQuest, Cleartool, Citrix, RPM (Resource Power Management), PMIC, Xerxes power controller and monitor system, CDP (Core Development Platform), and TCU (Temperature Controller Unit).
- Troubleshooting, debugging and analyzing PVT (Power, Voltage and Temperature) tests.
- Learned many complicated aspects of cellular phone blocks, systems and related development tools.

Senior Hardware Design Engineer – Contract Position – Nordson, Carlsbad, CA. Jan. 2012 – Aug. 2012

- Wrote VHDL and Verilog for Xilinx Spartan6 FPGA.
- Synthesized, implemented, and programmed FPGA in ISE, and performed Floor planning, layout, PAR and verification of module blocks.
- Simulated HDL in ModelSim PE and used Chipscope for debugging through Xilinx JTAG Interface. Designed FPGA circuits. Created and managed PCB and Schematic library components in Altium Designer IDE. Generated component footprints and schematic symbols.
- Created PCB layout, and implemented routing, part placement, back annotation, cross-probing. Generated output and Gerber files. Defined board shape, keepouts, layer stacks, high speed differential signal routing and tuning, and design rules.
- Created projects, workspace and SVN subversion version control. Managed document and design file control within embedded SVN control.
- Created components and views in 3D. Inspected and verified board and layout in 3D view.
- Debugged, verified and tested prototype board, using oscilloscope and logic Analyzer, JTAG dongle and debugger. Implemented, tested and verified Ethernet/EtherCAT IP core and automation control system through Beckhoff TwinCat hardware and software interface.

Senior FPGA Design Engineer – Contract Position – Ethercomm, Carlsbad, CA, Feb. 2011 – Sep. 2011

- Developed and designed Altera Cyclone IV GXB FPGA system in Quartus II environment for RF Radio Transceiver with high speed LVDS RFCB (RF Control Bus) interface.
- Created NIOS II, code memory, FLASH, SPI, USB and I/O interfaces with Avalon bus in SOPC Builder. Generated new interfaces in Component Editor. Wrote VHDL, Test Bench and TCL scripts for simulation in ModelSim. Debugged the design in real time using USB-Blaster with SignalTap and EDS debugger. Wrote operating system, control and monitoring 'C' functions and routines in EDS environment for NIOS II processor and created interrupt routines in 'C'.
- Generated HAL API BSF and FLASH programming files from sof. Programmed EPCS using synthesis sof and jic outputs, SFL and Quartus programmer. Designed and developed SLS USB using UTMI and ULPI interface.
- Designed FPGA schematic in PADS and wrote related VHDL hardware.

Senior FPGA Design Engineer – Contract Position – Curtiss-Wright, San Diego, CA, May. 2008 – Aug. 2010

- Developed VHDL & Verilog modules in ISE 11 for Xilinx Virtex5 FPGA. Created Testbench and simulated the design using ModelSim pe 6.5, and TCL (Tool Command Language) scripts. Used Vsim, Vcom and Vlog in TCL and Do commands. Created and managed libraries.
- Tools used in development: Coregen, iMPACT, PACE, Wave, Stimuli, ucf, JTAG, Emacs editor, Teraterm terminal, putty, Reflection Linux bridge, SAP document system.
  The following are a brief description of the modules and materials I have worked with:
- HDK (Hardware Development Kit), I2C, Config EEPROM, PLDA BFM (Bus Functional Model), GTP PCI express x8 and MGT PCIx, Link Core, SERDES, DMA controller and FIFO, FusionXF Capability, sFPDP (serial Front Panel Data Port) Fiber channels, DDRII SDRAM, TX & RX FIFO, vm V-Metro library and modules, BSIP (Board Support Intellectual Property), PMC (Processor Mezzanine Card), XMC, ADC512 AD Converter FMC (VITA 57.1 FPGA Mezzanine Card), 1000MSPS FMC-520 DA Converter, LVDS RIO (Rocket I/O) Interface, FPE320 3U VPX FPGA Processor Mezzanine site, HSS Diff.Pairs, backplane.
- FPGA programming in ISE through Xilinx Parallel Interface Cable IV, and test of JSM module by Xilinx iMPACT, CorEdge BIOS debugger, Intel 82571 Gigabit Ethernet Controller, JTAG chain.

Senior Firmware Engineer – Contract Position – Luxtera Inc., Carlsbad, CA, Sep. 2006 – May 2008

- Developed firmware in IAR Embedded System IDE for AT91SAM7S256 ARM7 based controller, used in

10 GBPS optical system. Wrote 'C', and Assembly routines for isr, SSC, SPI, 1Wire Temp. Sensor, QSFP I/F, Flash loader, parsing, .mac, cStartup, UART, I2C Master/Slave. Used Mathlab and LabView during the development. Worked with SAM-BA, configuration, debugger, Jlink JTAG ICE I/F, CSPY, XLINK.

- Developed QSFP and I2C slave Verilog code in ISE for Xilinx Spartan3.

Senior HW and Firmware design Engineer – Direct Position – General Atomics, Jan. 2005 – Oct. 2006

- Designed and developed 12 layer AT92RM9200 ARM9 based controller board with 180MHz PLL, interfacing 580MHz A/D and UWB RX/TX using PCAD 2004. Code development, ARM9 debugging and programming using Microcross X-Tools Compiler, Linker, GNU "as" Assembler, Make, Script, Signum JTAGJET, Chameleon ICE and FLASH programmer.
- Incorporated the following modules, components and devices into the design: Xilinx Virtex IV FPGA, ARM9 controller, SDRAM, serial Asynchronous FLASH, parallel FLASH, SRAM, JPEG2000 controller, CCD timing controller and interface, Camera Link controller, Power Supply, USB I/F, RS232. Designed and developed VHDL modules for Virtex IV FPGA using ISE8, PACE and iMPACT programmer, Xilinx JTAG, Synplify, RTL synthesis, Timing analysis.
- Created system flowchart and block diagrams. Wrote specification documents, …

Matt Moshir

- Oceanside, CA, USA

Contact Information

- 43j-itg-v5x@mail.dice.com (Preferred)
- 6199173971 (Preferred)

Work History

Total Work Experience: 9 years

- **Engineer | Qualcomm**
  Jan 01, 2012 - Jan 01, 2014

- **Electrical Engineer | Nordson**
  Jan 01, 2012 - Jan 01, 2012

Education

- **Bachelors**, No Dates Provided | University of Science and Technology

Skills

- **fpga** | 15yrs | 2021
- **simulation** | 15yrs | 2021
- **vhdl** | 15yrs | 2021
- **xilinx** | 15yrs | 2021
- **rtl** | 15yrs | 2021
- **ethernet** | 12yrs | 2021
- **debugging** | 10yrs | 2021
- **embedded linux** | 10yrs | 2021
- **linux** | 10yrs | 2021
- **scripting** | 10yrs | 2021

- **tcl** | 10yrs | 2021
- **verilog** | 10yrs | 2021
- **serdes** | 8yrs | 2021
- **vivado** | 6yrs | 2021
- **programming** | 5yrs | 2021
- **avionics** | 4yrs | 2021
- **design engineering** | 15yrs | 2020
- **hardware development** | 15yrs | 2020
- **integrated circuit design** | 15yrs | 2020
- **logic analyzer** | 15yrs | 2020
- **digital circuit design** | 15yrs | 2020
- **microcontroller** | 15yrs | 2020
- **i2c** | 12yrs | 2020
- **spi** | 12yrs | 2020
- **ise** | 12yrs | 2020
- **asic** | 10yrs | 2020
- **mixed-signal integrated circuit** | 10yrs | 2020
- **pci express** | 10yrs | 2020
- **mentor graphics** | 8yrs | 2020
- **jtag** | 7yrs | 2020
- **ddr sdram** | 4yrs | 2020
- **circuit design** | 15yrs | 2017
- **altium designer** | 8yrs | 2017
- **arm** | 8yrs | 2017
- **c** | 8yrs | 2017
- **altium** | 8yrs | 2017
- **modelsim** | 6yrs | 2017
- **assembly** | 5yrs | 2017
- **graphics**

Work Preferences

- Likely to Switch: Most Likely
- Willing to Relocate: No
- Travel Preference: Up to 50%
- Preferred Location:
    - San Diego, CA, USA
- Work Authorization:
    - US
- Work Documents:
    - US Citizenship
- Security Clearance: No
- Third Party: No

- Employment Type:
    - Contract - W2
    - Contract to Hire - Independent
    - Full-time
    - Contract to Hire - W2
    - Part-time
    - Contract - Independent

Profile Sources

- Dice: https://www.dice.com/employer/talent/profile/7d4fc8aabd2031f171a4743af0cb9b22f60c47c9